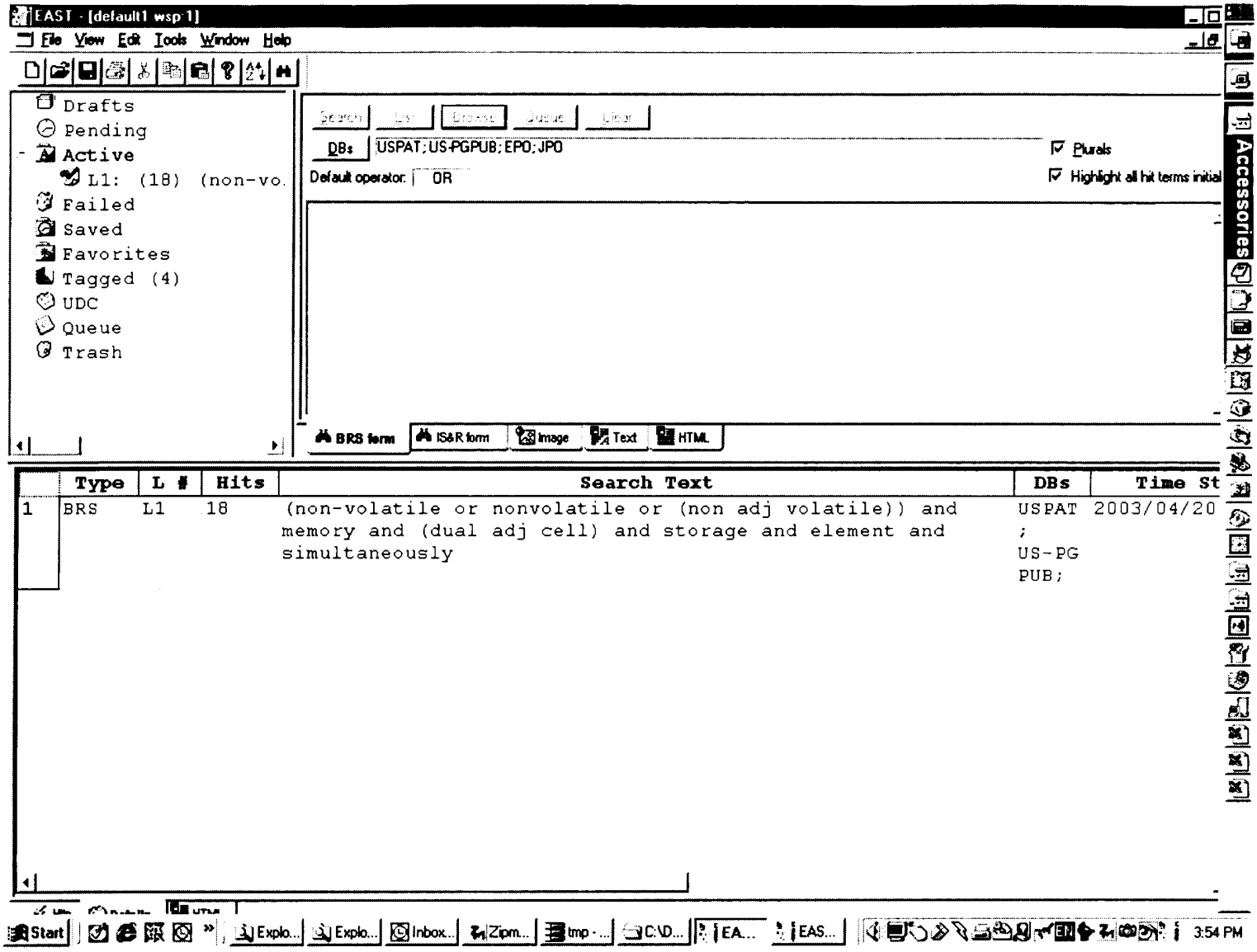
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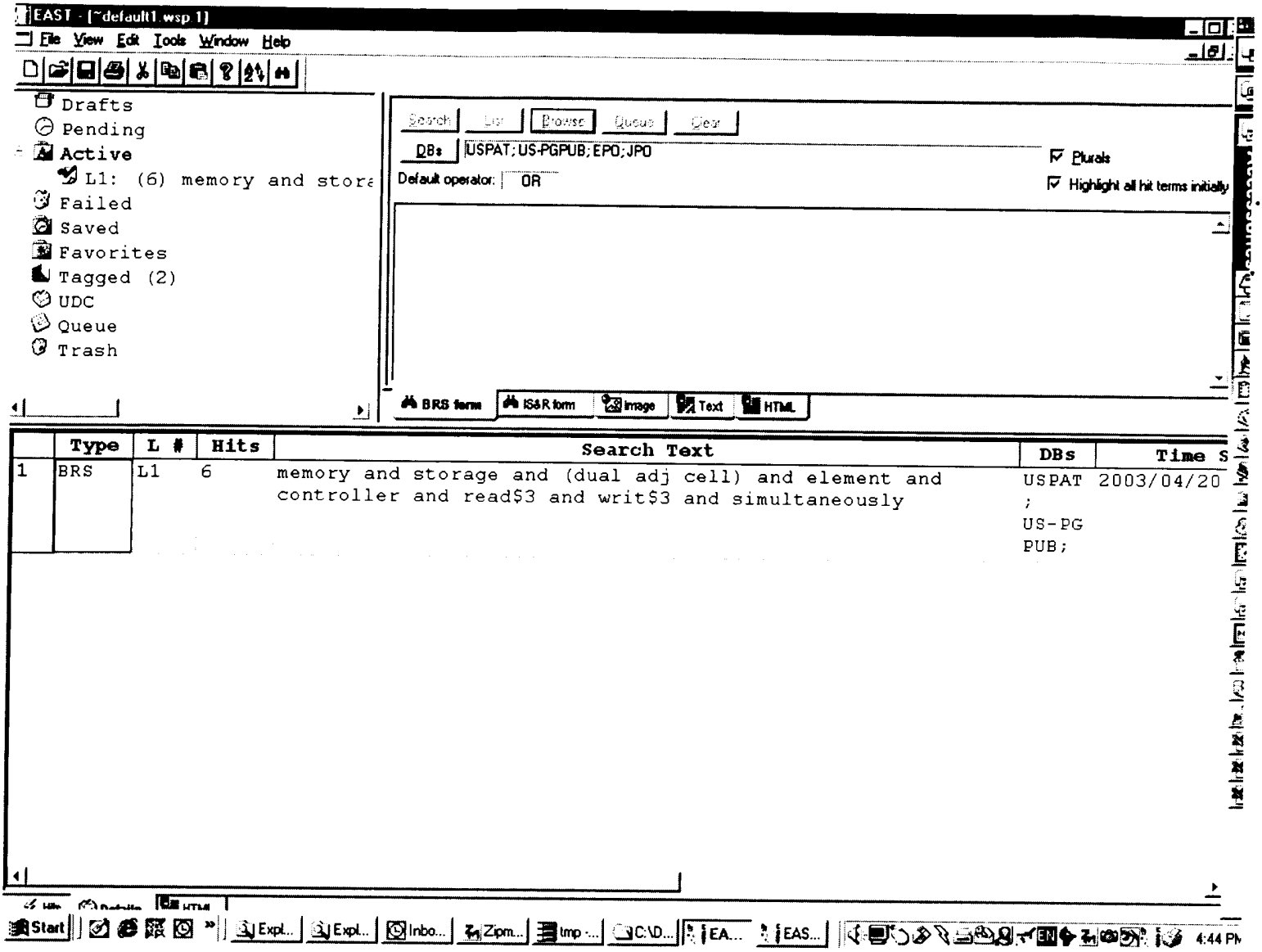
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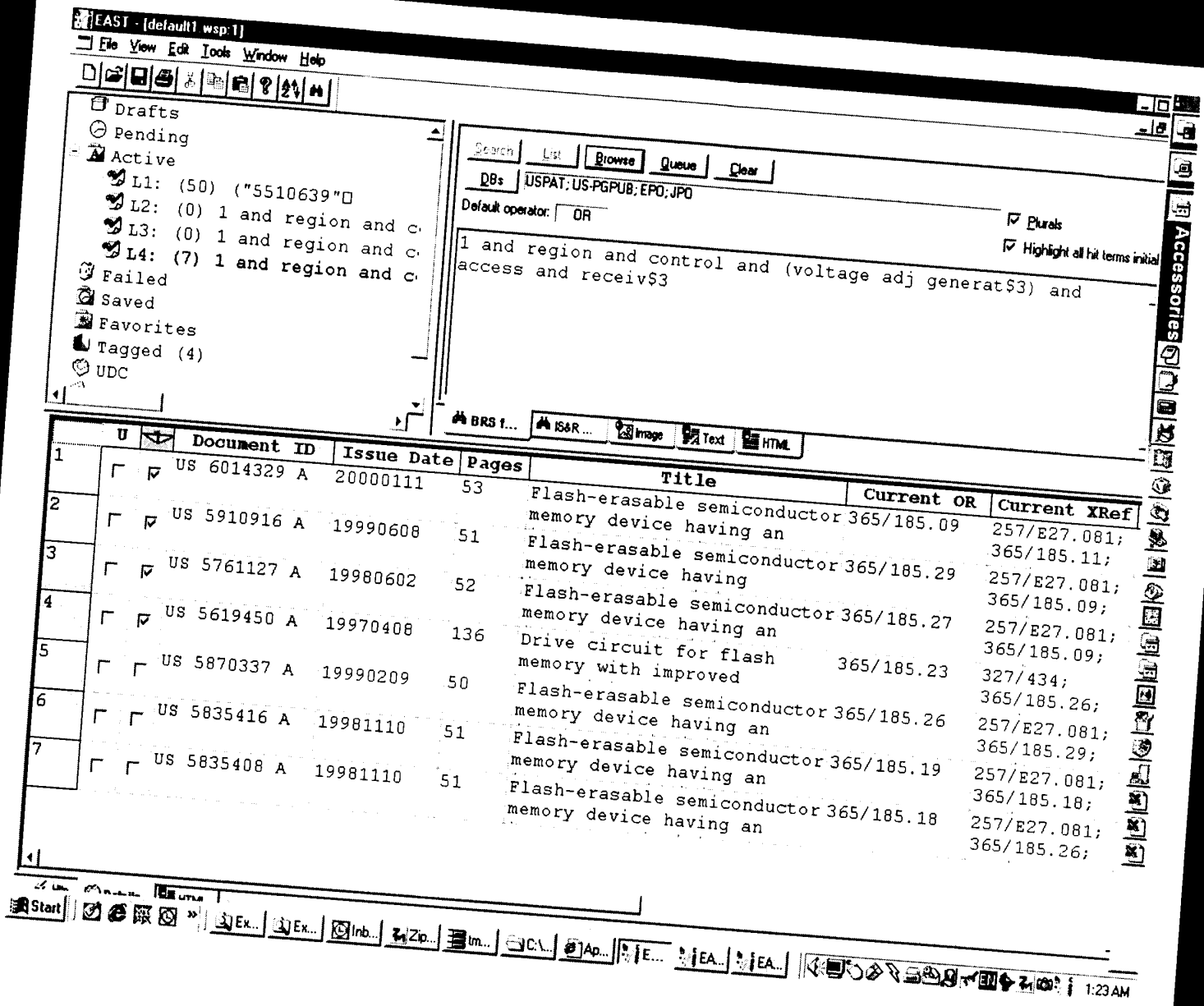
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1 US 6014329 A 20000111 53 Flash-erasable semiconductor memory device having an 365/185.09 257/E27.081; 365/185.11;
2 US 5910916 A 19990608 51 Flash-erasable semiconductor memory device having 365/185.29 257/E27.081; 365/185.09;
3 US 5761127 A 19980602 52 Flash-erasable semiconductor memory device having an 365/185.27 257/E27.081; 365/185.09;
4 US 5619450 A 19970408 136 Drive circuit for flash memory with improved 365/185.23 327/434; 365/185.26;
5 US 5870337 A 19990209 50 Flash-erasable semiconductor memory device having an 365/185.26 257/E27.081; 365/185.29;
6 US 5835416 A 19981110 51 Flash-erasable semiconductor memory device having an 365/185.19 257/E27.081; 365/185.18;
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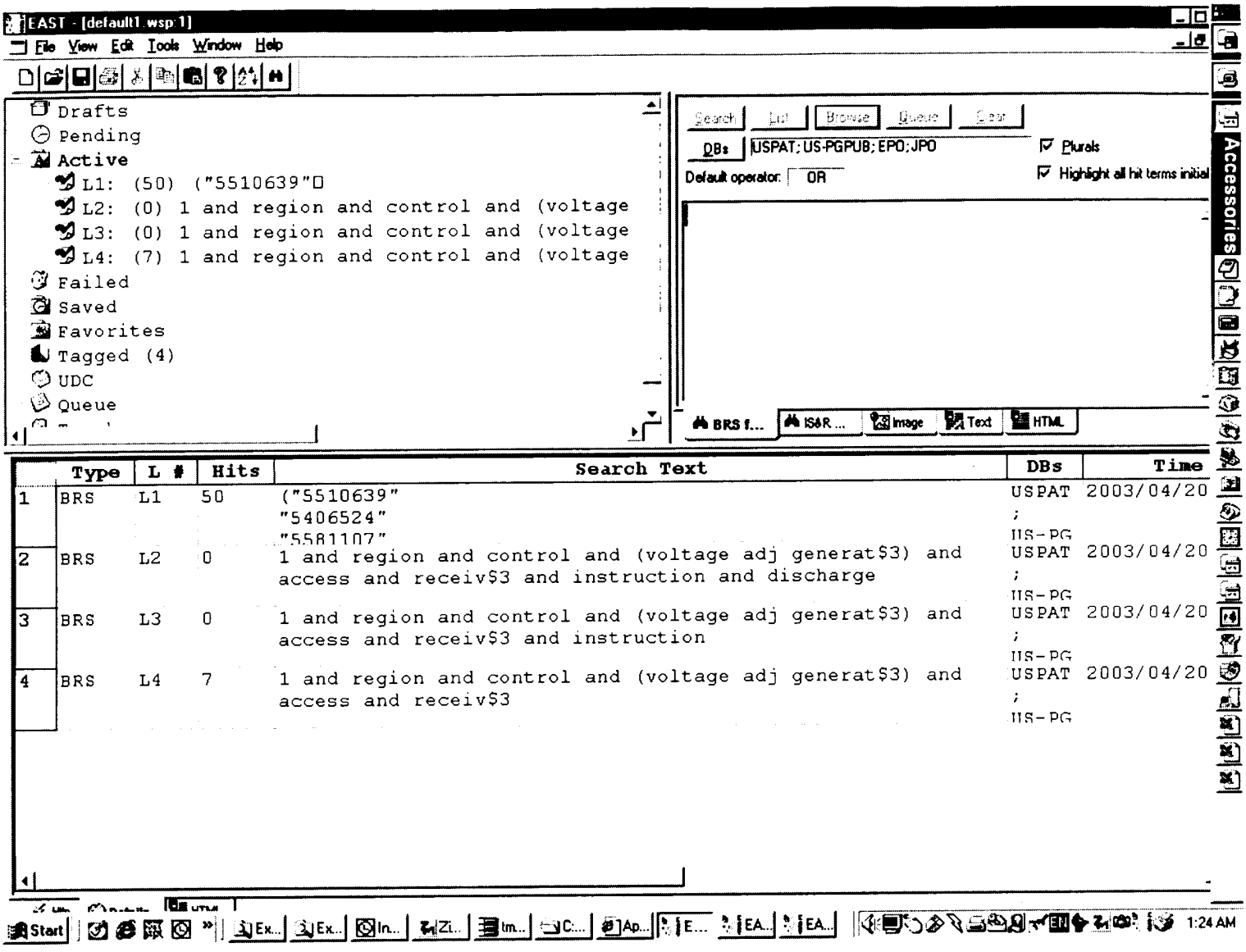

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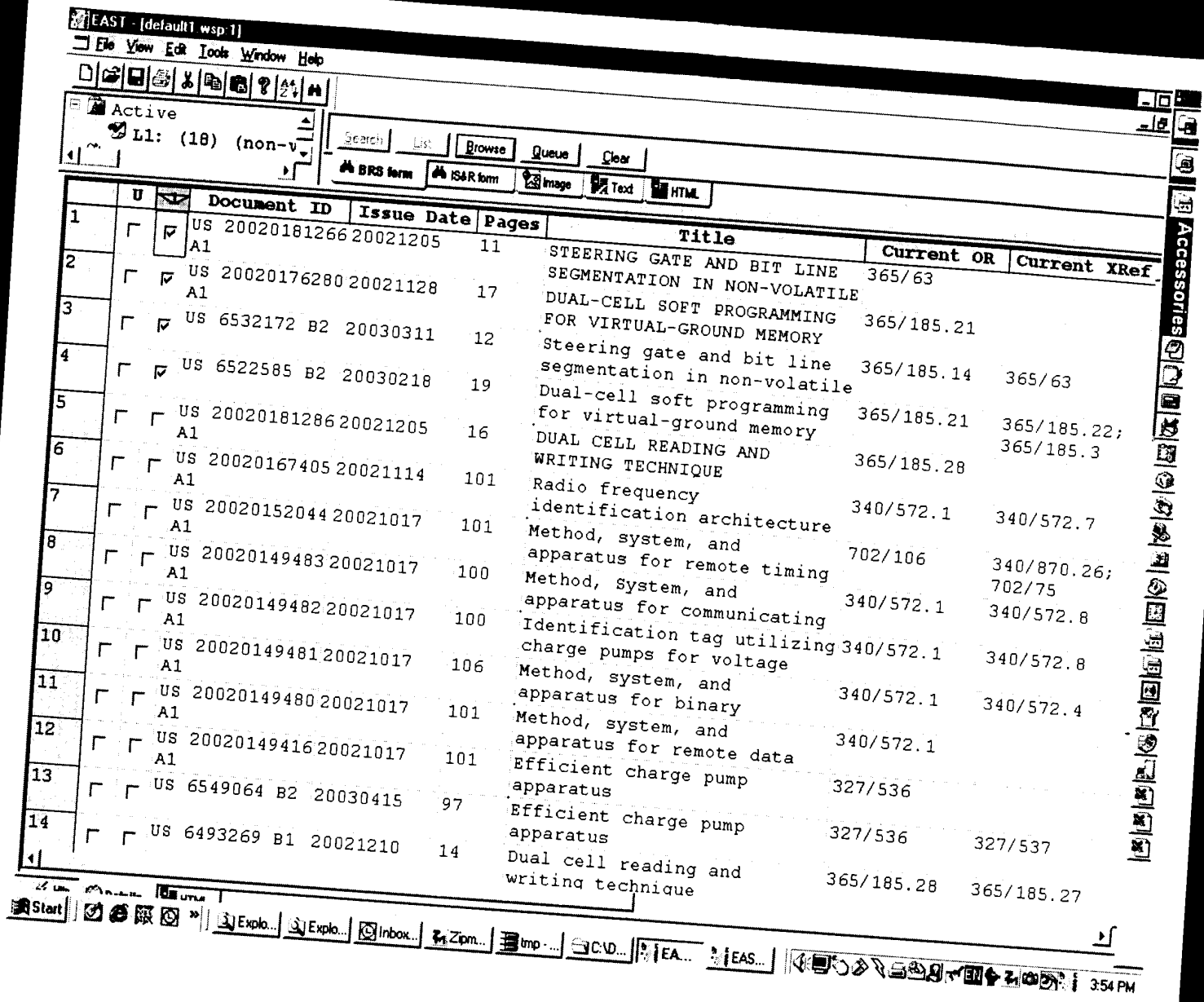

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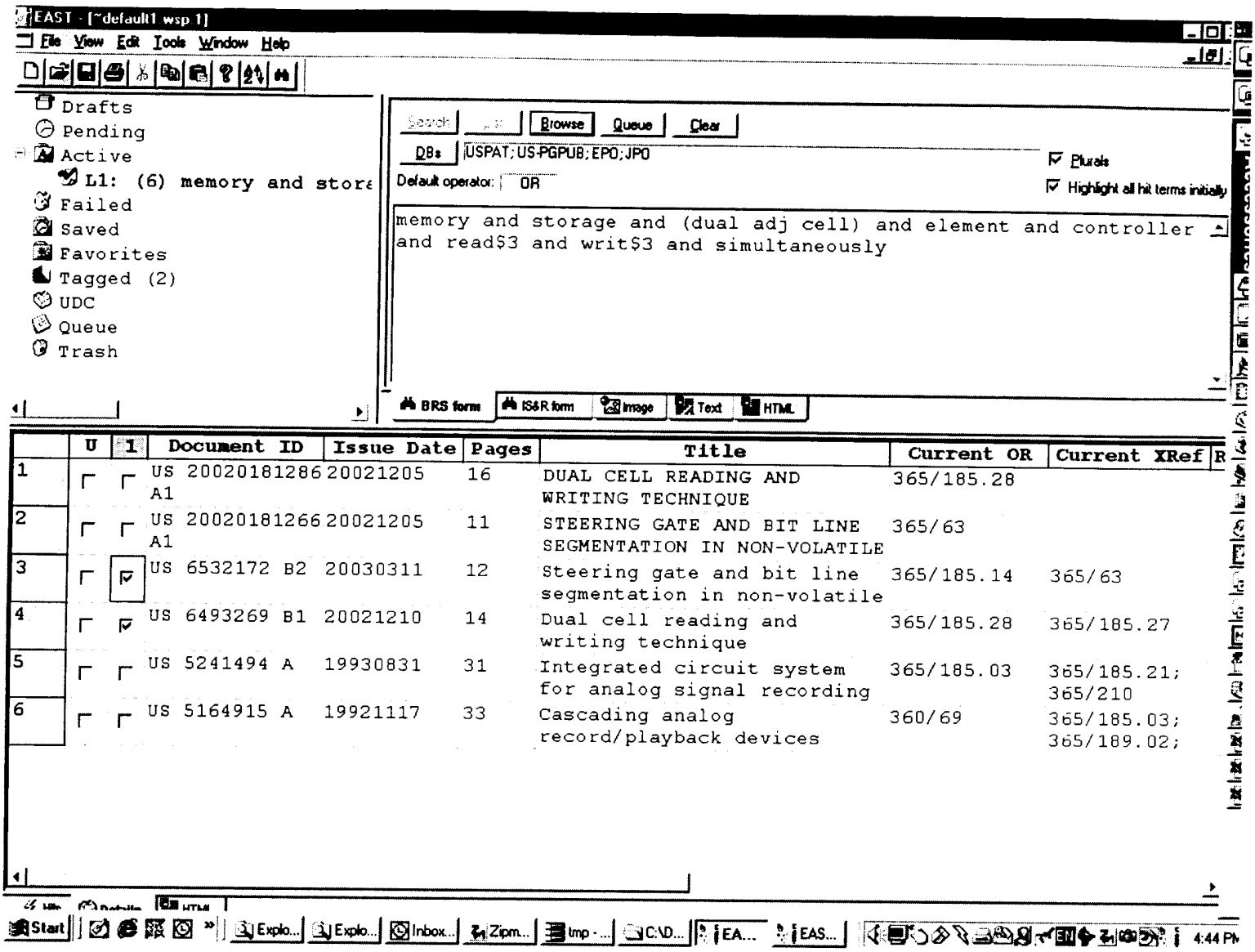
1	☐	☑	US 20020181266 A1	20021205	11	STEERING GATE AND BIT LINE SEGMENTATION IN NON-VOLATILE	365/63	
2	☐	☑	US 20020176280 A1	20021128	17	DUAL-CELL SOFT PROGRAMMING FOR VIRTUAL-GROUND MEMORY	365/185.21	
3	☐	☑	US 6532172 B2	20030311	12	Steering gate and bit line segmentation in non-volatile	365/185.14	365/63
4	☐	☑	US 6522585 B2	20030218	19	Dual-cell soft programming for virtual-ground memory	365/185.21	365/185.22; 365/185.3
5	☐	☐	US 20020181286 A1	20021205	16	DUAL CELL READING AND WRITING TECHNIQUE	365/185.28	
6	☐	☐	US 20020167405 A1	20021114	101	Radio frequency identification architecture	340/572.1	340/572.7
7	☐	☐	US 20020152044 A1	20021017	101	Method, system, and apparatus for remote timing	702/106	340/870.26; 702/75
8	☐	☐	US 20020149483 A1	20021017	100	Method, System, and apparatus for communicating	340/572.1	340/572.8
9	☐	☐	US 20020149482 A1	20021017	100	Identification tag utilizing charge pumps for voltage	340/572.1	340/572.8
10	☐	☐	US 20020149481 A1	20021017	106	Method, system, and apparatus for binary	340/572.1	340/572.4
11	☐	☐	US 20020149480 A1	20021017	101	Method, system, and apparatus for remote data	340/572.1	
12	☐	☐	US 20020149416 A1	20021017	101	Efficient charge pump apparatus	327/536	
13	☐	☐	US 6549064 B2	20030415	97	Efficient charge pump apparatus	327/536	327/537
14	☐	☐	US 6493269 B1	20021210	14	Dual cell reading and writing technique	365/185.28	365/185.27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2 US 20020181266 A1 20021205 11 STEERING GATE AND BIT LINE SEGMENTATION IN NON-VOLATILE 365/63
3 US 6532172 B2 20030311 12 Steering gate and bit line segmentation in non-volatile 365/185.14 365/63
4 US 6493269 B1 20021210 14 Dual cell reading and writing technique 365/185.28 365/185.27
5 US 5241494 A 19930831 31 Integrated circuit system for analog signal recording 365/185.03 365/185.21; 365/210
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(2) The various aspects of the present invention will be described with using more than one embodiment for the non-volatile memory cells composing the memory array. The initial discussion is based on the cell structure shown in FIGS. 3a and 3b. This is followed by a discussion using an array of memory cells with dual floating gates.

(3) The invention is directed to controlling programming current in a virtual-ground array memory architecture. The invention consists of circuitry to bias the array such that no source neighbors occur during soft programming. A feature of this bias configuration is that two cells are simultaneously soft-programmed. This dual-cell operation relies on the fact that neighbor cells will have very similar electrical characteristics and will therefore program at a similar rate. This is illustrated in FIG. 5, which is similar to FIG. 4 and depicts two groups of array cells (.alpha. and .beta.) within a larger array.

(4) FIG. 5 again shows a pair of words-lines, selected word-line WL.sub.0 520 and WL.sub.1 521 to represent the non-selected word-lines. Within an array, the cells are usually broken down into a number of groups of columns based on how the cells are simultaneously read and programmed, and which is reflected by the architecture used for the column decoders and sense amplifiers. In FIG. 5, the .alpha. cells and .beta. cells are two such groups which (along a given selected word-line) can be read and programmed separately and simultaneously.

(5) To avoid the sort of source-neighbor leakage described in the Background section and treat over-erased by soft programming, the non-volatile memory cells are soft-programmed in pairs. By biasing the bit-lines accordingly,, a pair of adjacent cells that shares a common source programmed together. In FIG. 5, cells .alpha..sub.2 and .alpha..sub.3 share a common source line BL.sub..alpha.2 512 for programming, with the current through both flowing out through current-limit circuit 531 to ground. The cells' respective drain lines, BL.sub..alpha.1 511 and BL.sub..alpha.3 513, are both set high, along with any of the drain neighbor bit-lines such as 510 and 514. This eliminates the uncontrolled source-neighbor current and the consequent problems that result. The combination of individual currents 501 and 503 is controlled by the current-limit circuit 531, these will generally be about the same value, but with that in the more over-erased cell slightly higher, as described below

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same way.

(16) This reduction of the number of lines is made possible when programming and reading functions, carried out in parallel on a number of floating gate storage elements that are spaced apart along a row of memory cells that is being accessed, apply common voltage conditions to the steering gates of all the spaced apart cells. It is normally desirable to minimize the number N of global steering lines used with a particular memory array. That minimum N depends upon the minimum spacing of memory cells along the rows that can be accessed at the same time for programming or reading. Typically, every fourth floating gate of the array of FIG. 3 may be accessed in parallel, for example, so it takes four such accesses, each with a different set of every fourth floating gate along the row, to perform the data programming or reading function on an entire row or contiguous segment of a row. During each of the four accesses, a different one of the lines 153 (FIG. 6) is enabled. If only every eighth floating gate may be simultaneously programmed or read, as another example, the number N of lines 153 becomes eight and every eighth one of the lines 151 is connected to a common one of the lines 153. The cells being programmed or read are spaced apart with one or several memory cells not being programmed or read being placed in between, as a way of minimizing pattern sensitive and/or disturb conditions. It is this consideration that influences the smallest N that may be employed in any specific memory arrangement.

(17) If the dual floating gate memory cell array of FIG. 4 is used in the segments 51', 52', 53' etc. instead of the single floating gate memory cell of FIG. 3, and N remains four, one pair of adjacent steering gates out of every four such pairs is connected in parallel. This is because each external steering gate line is connected to steering gates overlying two columns of floating gates in adjacent columns of cells. This allows the spacing of storage elements (floating gates) along a selected row that may be simultaneously programmed to be one in eight (one cell in four), or as dense as one floating gate in four, depending upon how the other array elements are driven in the particular programming method being used. One such method that allows one in three floating gates to be simultaneously programmed, with N then equaling three, is described in a patent application entitled "Dual Cell Reading and Writing Technique," filed concurrently herewith, naming Raul-Adrian Cernea as inventor, and assigned Ser. No. 09/871,332. This application is incorporated herein in its entirety by this reference.

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(13) Therefore, a solution to this problem of improving the control of the soft-programming current in a virtual ground arrays is needed.

(14) SUMMARY OF THE INVENTION

(15) The present invention is directed to controlling programming current in a virtual-ground array memory architecture. The invention consists of circuitry to bias the array such that no source neighbors occur during soft programming. A feature of this bias configuration is that two cells are simultaneously soft-programmed. This dual-cell operation relies on the fact that neighbor cells will have similar electrical characteristics and will therefore program at a similar rate.

(16) In one exemplary embodiment, the cells of the non-volatile memory array are programmed by a source side injection mechanism. Adjacent cells along a word-line share a common source line and are programmed together until one of the cells is verified to have the desired threshold value. The number of bit-lines between source lines can be as few as one, the actual drain required for programming. An additional means for controlling the soft-program rate is realized through the choice of the word-line voltage applied.

(17) Another exemplary embodiment uses memory cells with multiple floating gates. In this embodiment, the floating gate transistors within a cell are soft programmed separately from each other, but as part of a pair formed with a floating gate transistor in an adjacent cell.

(18) In any of the embodiments, more than one such pair, each from a separate block, may be soft-programmed simultaneously . The process can continue until either a first of these pairs, or until all of these pairs, no longer have both members of the pair over-erased.

(19) Additional aspects, features and advantages of the present invention are included in the following description of specific representative embodiments, which description should be taken in conjunction with the accompanying drawings.

DRAWING DESCRIPTION:

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that for soft programming a lower voltage is used. Instead of the 5-10 volts used for programming information, a voltage of less than 8 volts, and generally in the range of 0-2 volts is used.

(19) FIGS. 9a and 9b show dual-cell soft programming in a virtual-ground array 900 of dual floating gate memory cells. In FIG. 9a, the floating gate transistors .alpha..sub.0 and .alpha..sub.3 are being soft-programmed in a first group of cells along Select Line 0920. In similar manner, this can simultaneously be carried out in other groups of cells, such as the floating gates .beta..sub.0 and .beta..sub.3. Bit-line 912 is taken as the source and set to ground below the current limiter 931. The drains are then bit-lines 911 and 913, which, along with the drain neighbors such as 914, are set high. The control gate lines 942 and 943 on the source side of each of the cells are set at the overdrive voltage, here taken as 12 volts. This places the floating gate transistors .alpha..sub.0 and .alpha..sub.3 in an analogous situation to the cells .alpha..sub.2 and .alpha..sub.3 of FIG. 5. By selecting Select Line 0920, the currents 901 and 903 flow in the cells and the transistors .alpha..sub.0 and .alpha..sub.3 are programmed at the same time by applying the selected soft programming voltage along the Program Control Lines 941 and 944. Unlike FIG. 5, where the control gates of the cells .alpha..sub.0 and .alpha..sub.3 are connected, in more general embodiment the levels in lines 941 and 944 can be set separately, although here they are taken at the same value.

(20) As with the previous embodiment, in most cases it is preferable to continue the soft programming until a first one of the floating gate transistors in the pair verifies. Although these transistors are still in adjacent cells, the floating gate transistors themselves are not due to the intervening select transistors and the other floating gate transistors in the cell which are immediately adjacent to the source. These transistors will still be close enough so that process variations should be small, resulting in similar electrical characteristics and program rates. As the erase voltage variation along the select line will also be small over distance the order of a cell, both floating gate transistors in the soft programming pair will generally also have very similar threshold values at the end of an erase process and before the soft programming begins.

(21) Once a pair has finished soft programming, another pair in the group can be soft programmed. When the bit-line adjacent to a bit line which was

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